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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/014,359	12/14/2001	Michael Joachim Wolf	Q67426	1154

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EXAMINER	
JONES, PRENELL P	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/014,359	WOLF ET AL.	
	Examiner	Art Unit	
	Prenell P. Jones	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,5-8,12-17,19 and 20* is/are rejected.

7)☐ Claim(s) *2-4,9-11 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/19/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues on page 12 of response, that the cited prior art fails to teach or suggest phase matching between 2 delayed clock signals.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

2. Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, Applicant is claiming in line 4, "first and **second clock signal** and ***a second clock signal***," wherein it is unclear to Examiner as to what Applicant is claiming. Examiner question is "**second clock signal** and ***a second clock signal*** one in the same?

3. Claim 5 recites the limitation "***the respective selected***" in line 2 on page 4. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a

whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, 5-8, 12, 13-17, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakauchi et al (US Pat 5,455,840) in view and Mirov et al (US PAT. 6,845,457).

Regarding claims 1, 13-15 and 17, Nakauchi discloses phase compensation circuit/phase compensation module wherein the architecture includes determining time for delay, variable delay circuit and delay circuit (first delay means and second delay means) as associated with an internal clock signal (reference clock) and external clock signal, phase compensation module (PLL), PLL synchronization, phase adjustment means, phase adjustment associated with external clock is supplied by reference clock, phase matching selector, delay circuit, PLL input clock (internal clock) and the output clock (external clock) of the phase compensation circuit are identical with each other (Abstract, Fig. 2, 3 and 6, col. 2, line 55-67, col. 3, line 10-67, col. 5, line 55-63, col. 6, line 24-60, col. 11, line 31-40). However, Nakauchi is silent on a first/second delay means and the second clock signal adapting to the phase of the delayed first clock. In a

phase compensation environment, Mirov discloses synchronizing a delayed clock B/second clock with a delayed clock a signal/first clock (col. 10, line 27-45). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement a first/second delay means as well as synchronizing a second clock based on a first clock as taught by Mirov with the teachings of Nakauchi for the purpose of further minimizing the latency of received data.

Regarding claim 6, as indicated above, Nakauchi discloses phase compensation circuit/phase compensation module wherein the architecture includes determining time for delay, variable delay circuit and delay circuit (first delay means and second delay means) as associated with an internal clock signal (reference clock) and external clock signal, phase compensation module (PLL), PLL synchronization, phase adjustment means, phase adjustment associated with external clock is supplied by reference clock, phase matching selector, delay circuit, PLL input clock (internal clock) and the output clock (external clock) of the phase compensation circuit are identical with each other. Nakauchi further discloses utilizing flip-flops in a phase adjustment environment wherein the flip-flops have clock outputs (master-slave) (Fig. 7 and 8).

Regarding claims 5 and 7, as indicated above, Nakauchi discloses phase compensation circuit/phase compensation module wherein the architecture includes determining time for delay, variable delay circuit and delay circuit (first delay means and second delay means) as associated with an internal clock signal (reference clock) and external clock signal, phase compensation module (PLL), PLL synchronization, phase adjustment means, phase adjustment associated with external clock is supplied by reference clock, phase matching selector, delay circuit, PLL input clock (internal clock) and the output clock (external clock) of the phase

compensation circuit are identical with each other. Nakauchi further discloses a selector, which enables selecting between one of two clocks in a delayed environment (Figs. 3 and 6, col. 3, line 33-67).

Regarding claim 8 and 16, as indicated above, Nakauchi discloses phase compensation circuit/phase compensation module wherein the architecture includes determining time for delay, variable delay circuit and delay circuit (first delay means and second delay means) as associated with an internal clock signal (reference clock) and external clock signal, phase compensation module (PLL), PLL synchronization, phase adjustment means. Nakauchi further discloses outputting two clocks (Fig. 7 and 11, col. 11, 1-67).

Regarding claims 19 and 20, as indicated above, Nakauchi discloses that a first clock and second clock of the phase compensation circuit are identical with each other (col. 11, line 30-40).

Regarding claim 12, as indicated above, Nakauchi discloses phase compensation circuit/phase compensation module wherein the architecture includes determining time for delay, variable delay circuit and delay circuit (first delay means and second delay means) as associated with an internal clock signal (reference clock) and external clock signal, phase compensation module (PLL), PLL synchronization, phase adjustment means, phase adjustment associated with external clock is supplied by reference clock, phase matching selector, delay circuit, PLL input clock (internal clock) and the output clock (external clock) of the phase compensation circuit are identical with each other (Abstract, Fig. 2, 3 and 6, col. 2, line 55-67, col. 3, line 10-67, col. 5, line 55-63, col. 6, line 24-60, col. 11, line 31-40). However, Nakauchi is silent on compensation

module implementing phase adjustment via program code with respect to control means. In a phase compensation environment, Mirov discloses synchronizing a delayed clock B/second clock with a delayed clock a signal/first clock (col. 10, line 27-45). Nakauchi further discloses hardware and software associated with compensation environment, and a controller that executes software that implements phase adjustment (Fig. 11, col. 7, line 27-67). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be motivated to implement software/algorithms on hardware (first/second delay and phase adjuster) as taught by Mirov with the teachings of Nakauchi for the purpose of further managing compensation phase as associated with system clocks.

Allowable Subject Matter

4. Claims 2-4, 9-11 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: Although the combined cited art discloses phase compensation associated in a telecommunication environment wherein utilization of a first/second delay unit along with corresponding first/second clock signals and associated delay time, and adjusting the phase, they fail to teach or suggest with respect to claim 2, the first delay time and/or a start value for the second delay time are predetermined as a function of a maximum expected phase difference between the at least one first clock signal and the second clock signal and/or as a function of a maximum expected propagation time difference, which is caused by the transmission paths of different lengths, with respect to claims 3 and 4, first delay time corresponds to a maximum expected phase difference and/or maximum expected propagation

time difference between at least one first clock signal and the second clock signal, with respect to claim 9, the first or second start value is performed only upon attainment of a predetermined first deviation tolerance value, while the converse applies upon the attainment of a second deviation tolerance value which is smaller than the first deviation tolerance value, with respect to claims 10 and 11, phase adjustment changes the second delay time of second delay means in dynamic step sizes, a respective step size being modified as a function of the respective phase difference, regarding claim 18, code executed by control means on a console of a network device for a transmission with a SDH.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prenell P. Jones whose telephone number is 571-272-3180. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Prenell P. Jones

May 15, 2006

CHI PHAM
SUPERVISORY PATENT EXAM

5/15/06